BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Application of: Chow et al.

Serial No.: 09/884,660

Filed: June 19, 2001

Group Art Unit: 2663

Before the Examiner: Chang, Richard

Title: MAINTAINING SYNCHRONIZATION BETWEEN FRAME CONTROL WORD AND DATA FRAME PAIRS IN A HOME NETWORK

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

I. REAL PARTY IN INTEREST

The real party in interest is Advanced Micro Devices, Inc., which is the assignee of the entire right, title and interest in the above-identified patent application.

CERTIFICATION UNDER 37 C.F.R. §1.8

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Mail Stop Appeal Brief-Patents, Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450, on 3-15, 2006.

Toni Stanley
Signature

Toni Stanley
(Printed name of person certifying)

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences known to Appellants, Appellants' legal representative or assignee which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. STATUS OF CLAIMS

Claims 1-25 are pending in the Application. Claims 2-7 and 9-25 are allowed. Claims 1 and 8 stand rejected. Claims 1 and 8 are appealed.

IV. STATUS OF AMENDMENTS

Appellants have submitted an amendment on January 16, 2006 to rewrite objected claims 2 and 9 in independent form thereby allowing claims 2-7 and 9-14 following receipt of the final rejection with a mailing date of November 28, 2005.

V. SUMMARY OF CLAIMED SUBJECT MATTER

In one embodiment of the present invention, a method for maintaining synchronization in a home network that includes a host Ethernet media controller and an HPNA chip, where control frame and data frame pairs are transferred between the host Ethernet media access controller (MAC) and the HPNA chip, may comprise the step of sending a null frame from the host Ethernet MAC to the HPNA chip prior to the data frame. Specification, page 6, line 4 – page 7, line 18; Figure 1, elements 100, 112; Figure 2, elements 120, 122; Figure 3, element 140. The method may further comprise recognizing the null frame on the HPNA chip as an indication that a next received frame will be the data frame, thereby maintaining synchronization between the control frame and the data frame pairs. Specification, page 6, line 4 – page 7, line 18; Figure 1, element 100; Figure 2, elements 120, 122; Figure 3, element 140.

In another embodiment, a system for maintaining synchronization in a home network that includes a host Ethernet media access controller and an HPNA chip, where control frame and data frame pairs are transferred between the host Ethernet media access controller (MAC) and the HPNA chip, may comprise means for sending a null frame from the host Ethernet MAC to the HPNA chip prior to the data frame. Specification, page 6, line 4 – page 7, line 18; Figure 1, elements 100, 112; Figure 2, elements 120, 122; Figure 3, element 140. The system may further comprise means for recognizing the null frame on the HPNA chip as an indication that a next received frame will be the data frame, thereby maintaining synchronization between the control frame and the data frame pairs. Specification, page 6, line 4 – page 7, line 18; Figure 1, element 100; Figure 2, elements 120, 122; Figure 3, element 140.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Claims 1 and 8 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Holloway et al. (U.S. Patent No. 6,747,996) (hereinafter "Holloway").

VII. ARGUMENT

The Examiner has rejected claims 1 and 8 under 35 U.S.C. §103(a) as being unpatentable over Holloway. Office Action (11/28/2005), page 4. Appellants respectfully traverse these rejections for at least the reasons stated below.

A. Holloway does not teach or suggest the following claim limitations in claims 1 and 8.

Appellants respectfully assert that Holloway does not teach or suggest "a host Ethernet media controller and an HPNA chip" as recited in claim 1 and similarly in claim 8. The Examiner cites element 52 of Holloway as teaching a host Ethernet media controller and element 46b of Holloway as teaching an HPNA chip. Office

Action (11/28/2005), page 4. Appellants respectfully traverse the assertion that Holloway teaches the above-cited claim limitation. Instead, Holloway teaches a telephone handset connected to a terminal which consists in part of a voice codec which converts between analog signals and sampled data signals at a sample rate as well as consists of a HPNA network interface 46a which assembles the voice samples into a packet which is then transmitted on an HPNA network to a gateway. Column 2, lines 29-36. Holloway further teaches that the gateway receives a HPNA packet at the counterpart HPNA network I/F 46b and queues it for transmission by Wide Area Network (WAN) interface 52. Column 2, lines 36-39. There is no language in Holloway that describes a wide area network interface as being equivalent to a host Ethernet media access controller as asserted by the Examiner. The Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that WAN interface 52 teaches a host Ethernet media access controller. *See Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that WAN interface 52 teaches a host Ethernet media access controller, and that it would be so recognized by persons of ordinary skill. *See In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Since the Examiner has not provided such evidence, the Examiner is merely relying upon his own subjective opinion which is insufficient to establish a *prima facie* case of obviousness. *See In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002); M.P.E.P. §2143. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 1 and 8, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

The Examiner, in response to Appellants' above argument, states:

> The limitation of that Holloway does not teach or suggest 'a host Ethernet media controller and an HPNA chip,' Holloway further teaches that the DOCSIS compliant WAN interface (52) performs the

> MAC function connecting the HPNA interface (50) (See Fig. 3, Col. 2, lines 36-39), thus teaches all the functions for 'a host Ethernet media controller and an HPNA chip.' Office Action (11/28/2005), page 2.

Appellants respectfully traverse the assertion that column 2, lines 36-39 of Holloway teaches that WAN interface 52 performs MAC functions. As stated above, Holloway instead teaches that the gateway receives a HPNA packet at the counterpart HPNA network I/F 46b and queues it for transmission by Wide Area Network (WAN) interface 52. Column 2, lines 36-39. There is no language in the cited passage that WAN interface 52 performs MAC functions. A media access controller provides data link layer connectivity for local area network protocols, e.g., Ethernet. See www.wikipedia.com for definition of media access controller. The media access controller creates the Ethernet packets from the higher level network protocol packets. See www.wikipedia.com for definition of media access controller. Neither is there any language in the cited passage that WAN interface 52 performs the functions of the host Ethernet media access controller as described in the Specification. Hence, the Examiner has not provided extrinsic evidence that makes clear that WAN interface 52 teaches a host Ethernet media access controller, and that it would be so recognized by persons of ordinary skill. As stated above, the Examiner must provide extrinsic evidence that makes clear that WAN interface 52 teaches a host Ethernet media access controller, and that it would be so recognized by persons of ordinary skill. *See In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Since the Examiner has not provided such evidence, the Examiner is merely relying upon his own subjective opinion which is insufficient to establish a *prima facie* case of obviousness. *See In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002); M.P.E.P. §2143. Consequently, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 1 and 8, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Appellants further assert that Holloway does not teach or suggest "wherein control frame and data frame pairs are transferred between the host Ethernet media access controller (MAC) and the HPNA chip" as recited in claim 1 and similarly in claim 8. The Examiner cites Figure 17 and column 3, lines 11-13 of Holloway as teaching the above-cited claim limitation. Office Action (11/28/2005), page 4. Appellants respectfully traverse.

Holloway instead teaches that a synchronization protocol is established between a synchronous terminal and a synchronous end point by providing a gateway between the asynchronous communications network and the synchronous end point. Column 3, lines 5-8. Holloway further teaches that the gateway communicates with the synchronous terminal over the asynchronous communications network in accordance with the synchronization protocol. Column 3, lines 8-11. Holloway further teaches that the synchronization protocol includes sending a message (referred to as the "SP packet") from the gateway to the synchronous terminal where the SP packet contains a timestamp identifying a clock associated with the synchronous end point. Column 3, lines 11-15. Hence, Holloway teaches sending a packet that contains a timestamp from the gateway to the synchronous terminal.

The Examiner has not provided any evidence that the SP packet that contains a timestamp discloses a control frame or a data frame or a control fame and data frame pair. The Examiner must provide a basis in fact and/or technical reasoning to reasonably support the determination that the SP packet that contains a timestamp teaches a control frame or a data frame or a control fame and data frame pair. *See Ex parte Levy*, 17 U.S.P.Q.2d 1461, 1464 (Bd. Pat. App. & Inter. 1990). That is, the Examiner must provide extrinsic evidence that must make clear that the SP packet that contains a timestamp teaches a control frame or a data frame or a control fame and data frame pair, and that it would be so recognized by persons of ordinary skill. *See In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999). Since the Examiner has not

provided such evidence, the Examiner is merely relying upon his own subjective opinion which is insufficient to establish a *prima facie* case of obviousness. *See In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002); M.P.E.P. §2143. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 1 and 8, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Furthermore, in connection with the rejection of the claim limitation recited in the above paragraph, the Examiner cites to the voice packet disclosed in Figure 17 as teaching a data frame and to the SP packet disclosed in Figure 17 as teaching a control frame. Office Action (11/28/2005), page 4. The Examiner has not provided any evidence that the SP packet and voice packet are pairs as required by the language recited in the above-recited claim limitation. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 1 and 8, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

In response to Appellants' above argument, the Examiner asserts that the SP packet is the control fame and that the voice packet is the data frame. Office Action (11/28/2005), page 3. The Examiner further cites column 8, lines 22-49 of Holloway as teaching the above-cited claim limitation. Office Action (11/28/2005), page 3. Appellants respectfully traverse. Holloway instead teaches that the frame commences with null data or padding to fill out the frame to reach the synchronization time, and then has the voice sample packet at the very end and the rest of the frame. Column 8, lines 32-35. Holloway further teaches that this way, the active packetized voice stations ensure there is no basic access delay, since the end of the first voice packet occurs at a predictable time. Column 8, lines 36-38. Hence, Holloway teaches that a frame is padded with null data, as illustrated in Figure 17, in order to eliminate "basic access delay" (referring to the delay from T0 to when the currently active station (if

any) finishes its transmission). This padding of null data either fills out the frame or commences the frame. It is used to effectively ensure the length of the frame has a particular length. The null data is not a separate frame that is sent from the host Ethernet MAC to the HPNA chip prior to the data frame. Instead, the null data fills out the frame just prior to the SP packet as illustrated in Figure 17. There is no language in the cited passage that teaches that the SP (synchronization protocol) packet is equivalent to a control frame, as defined in the Specification[1]. For example, the control fame may contain a frame control word. Specification, page 5, lines 4-11. Hence, there is no language in the cited passage that teaches control frame and data frame pairs. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 1 and 8, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Appellants further assert that Holloway does not teach or suggest "sending a null frame from the host Ethernet MAC to the HPNA chip prior to the data frame" as recited in claim 1 and similarly in claim 8. The Examiner cites Figure 17 and column 8, lines 3-7 of Holloway as teaching the above-cited claim limitation. Office Action (11/28/2005), page 4. Appellants respectfully traverse and assert that Holloway instead teaches that if three packetized voice stations are active, then the gateway would signal in the SP packet that station 1 should preload its Backoff Level (BL) with 1, that station 2 should preload with 0 and that station 3 should preload with 2. There is no language in the cited passage that teaches sending a null frame. Neither is there any language in the cited passage that teaches sending a null frame from a host Ethernet MAC to the HPNA chip. Neither is there any language in the cited passage that teaches sending a null frame from the host Ethernet MAC to the HPNA chip prior to a data frame. Therefore, the Examiner has not presented a *prima facie*

[1] The specification can be used as a dictionary to learn the meaning of a term in the patent claim. *Toro*

case of obviousness in rejecting claims 1 and 8, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

In response to Appellants' above argument, the Examiner asserts that the SP packet is the control fame and that the voice packet is the data frame. Office Action (11/28/2005), page 3. The Examiner further cites to column 8, lines 22-49 of Holloway as teaching the above-cited claim limitation. Office Action (11/28/2005), page 3. Appellants respectfully traverse. Holloway instead teaches that the frame commences with null data or padding to fill out the frame to reach the synchronization time, and then has the voice sample packet at the very end and the rest of the frame. Column 8, lines 32-35. Holloway further teaches that this way, the active packetized voice stations ensure there is no basic access delay, since the end of the first voice packet occurs at a predictable time. Column 8, lines 36-38. Hence, Holloway teaches that a frame is padded with null data, as illustrated in Figure 17, in order to eliminate "basic access delay" (referring to the delay from T0 to when the currently active station (if any) finishes its transmission). This padding of null data either fills out the frame or commences the frame. It is used to effectively ensure the length of the frame has a particular length. The null data is not a separate frame that is sent from the host Ethernet MAC to the HPNA chip prior to the data frame. Instead, the null data fills out the frame just prior to the SP packet as illustrated in Figure 17. Hence, the cited passage does not teach sending a null frame from the host Ethernet MAC to the HPNA chip prior to the data frame. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 1 and 8, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

Co. v. White Consol. Indus., Inc., 199 F.3d 1295, 1299, 53 U.S.P.Q.2d 1065, 1067 (Fed. Cir. 1999).

Appellants further assert that Holloway does not teach or suggest "recognizing the null frame on the HPNA chip as an indication that a next received frame will be the data frame, thereby maintaining synchronization between the control frame and the data frame pairs" as recited in claim 1 and similarly in claim 8. The Examiner cites Figure 17 and column 8, lines 3-7 of Holloway as teaching the above-cited claim limitation. Office Action (11/28/2005), page 4. Appellants respectfully traverse. As stated above, Holloway instead teaches that if three packetized voice stations are active, then the gateway would signal in the SP packet that station 1 should preload its Backoff Level (BL) with 1, that station 2 should preload with 0 and that station 3 should preload with 2. There is no language in the cited passage that teaches sending a null frame. Neither is there any language in the cited passage that teaches recognizing the null frame on an HPNA chip. Neither is there any language in the cited passage that teaches recognizing the null frame on a HPNA chip as an indication that a next received frame will be the data frame. Neither is there any language in the cited passage that teaches maintaining synchronization between the control frame and the data frame pairs. Therefore, the Examiner has not presented a *prima facie* case of obviousness in rejecting claims 1 and 8, since the Examiner is relying upon an incorrect, factual predicate in support of the rejection. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1455 (Fed. Cir. 1998).

In response to Appellants' above argument, the Examiner states that the Specification discloses that the null frame is a control frame and hence concludes that Holloway teaches the above-cited claim limitation. Office Action (11/28/2005), page 3. Appellants do not understand how this illustrates that Holloway discloses the above-cited claim limitation. The claim recites that the null frame is recognized on the HPNA chip as an indication that a next received frame will be the data frame thereby maintaining synchronization between the control and the data frame pairs. The Examiner must show that Holloway teaches or suggests this claim limitation in order to establish a *prima facie* case of obviousness. M.P.E.P. §2143. Since the

Examiner has not shown that Holloway teaches or suggests this claim limitation, the Examiner has not established a *prima facie* case of obviousness in rejecting claims 1 and 8. *Id.*

B. The Examiner's motivation is insufficient to establish a *prima facie* case of obviousness.

Most if not all inventions arise from a combination of old elements. *See In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457 (Fed. Cir. 1998). Obviousness is determined from the vantage point of a hypothetical person having ordinary skill in the art to which the patent pertains. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1457 (Fed. Cir. 1998). Therefore, an Examiner may often find every element of a claimed invention may often be found in the prior art. *Id.* However, identification in the prior art of each individual part claimed is insufficient to defeat patentability of the whole claimed invention. *See Id.* In order to establish a *prima facie* case of obviousness, the Examiner must show reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would select the elements from the cited prior art references for combination in the manner claimed. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998). That is, the Examiner must provide some suggestion or motivation, either in the references themselves, the knowledge of one of ordinary skill in the art, or, in some case, the nature of the problem to be solved, to modify the reference or to combine reference teachings. *See In re Dembiczak*, 175 F.3d 994, 999, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999). Whether the Examiner relies on an express or an implicit showing, the Examiner must provide particular findings related thereto. *In re Kotzab*, 55 U.S.P.Q.2d 1313, 1317 (Fed. Cir. 2000).

The Examiner admits that Holloway does not teach an HPNA chip, as recited in claims 1 and 8. Office Action (11/28/2005), page 5. The Examiner's motivation for modifying Holloway to include an HPNA chip is "for higher density and less chip count for the same function as the design trend in the industry since it has been held

by *In re Larson*, 340 F.2d 732, 93, 129 USPQ 23 (CCPA 1961)." Office Action (6/28/2005), page 3. The Examiner further states that the motivation for modifying Holloway to include an HPNA chip since it "is merely a matter of obvious engineering choice since it has been held by *In re Larson*, 340 F.2d 965, 968. [sic] 144 USPQ 347, 349 (CCPA 1965)." Office Action (11/28/2005), pages 2 and 5. The Examiner's motivation is insufficient to support a *prima facie* case of obviousness for at least the reasons stated below.

In order to establish a *prima facie* case of obviousness, the Examiner must provide some suggestion or motivation, either in the references themselves, the knowledge of one of ordinary skill in the art, or, in some cases the nature of the problem to be solved, to modify the reference or to combine reference teachings. *See In re Dembiczak*, 175 F.3d 1994, 999, 50 U.S.P.Q.2d 1614, 1617 (Fed. Cir. 1999). The Examiner has not provided any evidence that his motivation comes from any of these sources. Instead, the Examiner is relying upon his own subjective opinion which is insufficient to support a prima facie case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 1 and 8. *Id.*

The Examiner's motivation ("for higher density and less chip count for the same function as the design trend in the industry") does not provide reasons that the skilled artisan, confronted with the same problems as the inventor and with no knowledge of the claimed invention, would modify Holloway to include an HPNA chip. Accordingly, the Examiner has not presented a *prima facie* case of obviousness for rejecting claims 1 and 8. *In re Rouffet*, 47 U.S.P.Q.2d 1453, 1458 (Fed. Cir. 1998).

The Examiner's motivation ("for higher density and less chip count for the same function as the design trend in the industry") is not a motivation for modifying Holloway, which teaches synchronizing synchronous terminals with synchronous endpoints, each synchronous terminal and each synchronous endpoint having an asynchronous communications network coupled between at least one synchronous terminal and at least one synchronous endpoint (column 2, line 67 – column 3, line 5), to include an HPNA chip. The Examiner has failed to explain any rationale connection between having higher density and less chip count and modifying Holloway to have an HPNA chip. Further, the Examiner has failed to explain any connection between having higher density and less chip count and modifying Holloway to send a null frame from the host Ethernet MAC to the HPNA chip prior to a data frame, as recited in claims 1 and 8. Neither has the Examiner explained any connection between having higher density and less chip count and modifying Holloway to recognize the null frame on the HPNA chip as an indication that a next received frame will be the data frame, thereby maintaining synchronization between the control frame and the data frame pairs, as recited in claims 1 and 8. Instead, the Examiner is relying upon his own subjective opinion which is insufficient to support a prima facie case of obviousness. *In re Lee*, 61 U.S.P.Q.2d 1430, 1434 (Fed. Cir. 2002). Consequently, the Examiner's motivation is insufficient to support a *prima facie* case of obviousness for rejecting claims 1 and 8. *Id.*

C. *In re Larson* does not support modifying Holloway to include an HPNA chip.

As stated above (in Section B), the Examiner cited *In re Larson* for supporting the modification of Holloway to include an HPNA chip. Office Action (6/28/2005), page 3; Office Action (11/28/2005), pages 2 and 5. Appellants respectfully assert that *In re Larson* does not provide support for modifying Holloway to include an HPNA chip. The court in *In re Larson* construed the term "integral" in a claim to include the constituent parts of a brake disc and clamp. *In re Larson*, 144 U.S.P.Q. at

349. The court held that while the brake disc and clamp of reference comprise several parts, they are rigidly secured together as a single unit; constituent parts are so combined as to constitute a unitary whole, which is "integral" within meaning of claim. *Id.* The court continued by holding that the term "integral" is not limited to a fabrication of parts from a single piece of metal, but is inclusive of other means for maintaining parts fixed together as a single unit; moreover, use of a one piece construction instead of the reference structure is a matter of obvious engineering choice. *Id.* While the court concluded that under the facts presented in this particular case that the use of a one piece construction instead of the reference structure is a matter of obviousness choice, the Examiner has failed to provide any reasoning as to how this implies that the use of an HPNA chip in Holloway is simply a matter of obvious engineering choice. The court in *In re Larson* focused on interpreting the term "integral." Accordingly, the citing of *In re Larson* does not provide support for modifying Holloway to include an HPNA chip.

Further, if the Examiner is asserting that since Holloway teaches an HPNA interface 46b in gateway 50 that it would be an obvious engineering choice to use an HPNA chip in Holloway, then where would the HPNA chip be? Is the Examiner asserting that gateway 50 is the HPNA chip? Further, Holloway also teaches an HPNA interface 46a in terminal 42. Would the Examiner then be asserting that the HPNA chip is also terminal 42? These HPNA interfaces are used to interface the HPNA network with terminal 42 and gateway 50 as illustrated in Figure 3. Appellants respectfully assert that the Examiner has not shown that it would be an obvious engineering choice to have Holloway use an HPNA chip.

Further, Applicants note that *In re Larson*, upon which the Examiner relies, precedes *Graham v. John Deere Co.*, 383 U.S. 1, 148 U.S.P.Q. 459 (1966). Accordingly, the holdings of *Graham* may overrule the holdings of *In re Larson.*

VIII. CONCLUSION

For the reasons noted above, the rejections of claims 1 and 8 are in error. Appellants respectfully request reversal of the rejections and allowance of claims 1-25.

Respectfully submitted,
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CLAIMS APPENDIX

1. A method for maintaining synchronization in a home network that includes a host Ethernet media controller and an HPNA chip, where control frame and data frame pairs are transferred between the host Ethernet media access controller (MAC) and the HPNA chip, the method comprising the steps of:

(a) sending a null frame from the host Ethernet MAC to the HPNA chip prior to the data frame; and

(b) recognizing the null frame on the HPNA chip as an indication that a next received frame will be the data frame, thereby maintaining synchronization between the control frame and the data frame pairs.

2. A method for maintaining synchronization in a home network that includes a host Ethernet media controller and an HPNA chip, where control frame and data frame pairs are transferred between the host Ethernet media access controller (MAC) and the HPNA chip, the method comprising the steps of:

(a) sending a null frame from the host Ethernet MAC to the HPNA chip prior to the data frame; and

(b) recognizing the null frame on the HPNA chip as an indication that a next received frame will be the data frame, thereby maintaining synchronization between the control frame and the data frame pairs;

wherein the null frame includes a source address field and an Ethernet type field, step (a) further including the step of providing an invalid address in the source address field and the Ethernet type field.

3. The method of claim 2 wherein step (a) further includes the step of providing all-zeros in the source address field and the Ethernet type field.

4. The method of claim 2 wherein step (a) further includes the step of providing the null frame as a minimum size Ethernet frame.

5. The method of claim 2 wherein step (a) further includes the step of issuing from the host Ethernet MAC a minimum size frame containing a frame control word prior to the data frame during a transmit sequence.

6. The method of claim 2 wherein step (a) further includes the step of issuing from the HPNA chip a minimum size frame containing a frame status word with the data frame during a receive sequence.

7. The method of claim 2 wherein the null frame further includes a destination address field, step (a) further including the step of providing the destination address with a destination address of a corresponding frame received during a receive sequence.

8. A system for maintaining synchronization in a home network that includes a host Ethernet media access controller and an HPNA chip, wherein control frame and data frame pairs are transferred between the host Ethernet media access controller (MAC) and the HPNA chip, the system comprising:

(a) means for sending a null frame from the host Ethernet MAC to the HPNA chip prior to the data frame; and

(b) means for recognizing the null frame on the HPNA chip as an indication that a next received frame will be the data frame, thereby maintaining synchronization between the control frame and the data frame pairs.

9. A system for maintaining synchronization in a home network that includes a host Ethernet media access controller and an HPNA chip, wherein control frame and data frame pairs are transferred between the host Ethernet media access controller (MAC) and the HPNA chip, the system comprising:

(a) means for sending a null frame from the host Ethernet MAC to the

HPNA chip prior to the data frame; and

(b) means for recognizing the null frame on the HPNA chip as an indication that a next received frame will be the data frame, thereby maintaining synchronization between the control frame and the data frame pairs;

wherein the null frame includes a source address field and an Ethernet type field that contains an invalid address.

10. The system of claim 9 wherein the source address field and the Ethernet type field contain all-zeros.

11. The system of claim 9 wherein the null frame comprises a minimum size Ethernet frame.

12. The system of claim 9 wherein the host Ethernet MAC issues a minimum size frame containing a frame control word prior to the data frame during a transmit sequence.

13. The system of claim 9 wherein the HPNA chip issues a minimum size frame containing a frame status word with the data frame during a receive sequence.

14. The system of claim 9 wherein the null frame further includes a destination address field that contains a destination address of a corresponding frame received during a receive sequence.

15. A method for maintaining synchronization in a home network that includes a host Ethernet media access controller program and media interface of an HPNA chip, where control frame and data frame pairs are transferred between the host Ethernet media access controller (MAC) and the HPNA chip, the method comprising the steps of:

(a) sending a null frame having a source address field and an Ethernet type field from the host Ethernet MAC to the media interface prior to the data frame, wherein the source address field and the Ethernet type field in the null frame include all zeros; and

(b) in response to receiving the null frame by the media interface, recognizing the zeros in the source address field and the Ethernet type field as an indication that a next received frame will be the data frame, thereby maintaining synchronization between the control frame and the data frame pairs.

16. The method of claim 15 wherein step (a) further includes the step of providing the null frame as a minimum size Ethernet frame.

17. The method of claim 16 wherein step (a) further includes the step of issuing from the host Ethernet MAC the null frame containing a frame control word prior to the data frame during a transmit sequence.

18. The method of claim 17 wherein step (a) further includes the step of issuing from the HPNA chip the null frame containing a frame status word with the data frame during a receive sequence.

19. The method of claim 18 wherein the null frame further includes a destination address field, step (a) further including the step of providing the destination address with a destination address of a corresponding frame received during a receive sequence.

20. A home network, comprising:

a host Ethernet media access controller (MAC);

an HPNA chip having a media interface in communication with the host Ethernet MAC; and

control frame and data frame pairs transferred between the host Ethernet MAC and the HPNA chip, wherein the control frame includes a source address field and an Ethernet type field,

wherein synchronicity is maintained between the control frame and data frame pairs by placing an invalid address in the source address field and the Ethernet type field of the control frame, such that the invalid address indicates to a receiver of the control frame that a next received frame will be the data frame.

21. The system of claim 20 wherein the invalid address comprises all zeros.

22. The system of claim 20 wherein the null frame comprises a minimum size Ethernet frame.

23. The system of claim 21 wherein the host Ethernet MAC issues a minimum size frame containing a frame control word prior to the data frame during a transmit sequence.

24. The system of claim 22 wherein the HPNA chip issues a minimum size frame containing a frame status word with the data frame during a receive sequence.

25. The system of claim 23 wherein the null frame further includes a destination address field that contains a destination address of a corresponding frame received during a receive sequence.

EVIDENCE APPENDIX

No evidence was submitted pursuant to §§1.130, 1.131, or 1.132 of 37 C.F.R. or of any other evidence entered by the Examiner and relied upon by Appellants in the Appeal.

RELATED PROCEEDINGS APPENDIX

There are no related proceedings to the current proceeding.

PTO/SB/17 (11-04)
Approved for use through 07/31/2006. OMB 0651-0032
U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Effective on 10/01/2004. Patent fees are subject to annual revision.

FEE TRANSMITTAL
For FY 2005

☐ Applicant claims small entity status. See 37 CFR 1.27

TOTAL AMOUNT OF PAYMENT ($) **500.00**

Complete if Known	
Application Number	09/884,660
Filing Date	06/19/2001
First Named Inventor	Peter K. Chow
Examiner Name	Chang, Richard
Art Unit	2663
Attorney Docket No.	F1018

METHOD OF PAYMENT (check all that apply)

☐ Check ☐ Credit Card ☐ Money Order

☑ Deposit Account ☐ None

Deposit Account Number: 01-0365

Deposit Account Name: Advanced Micro Devices, Inc.

The Director is hereby authorized to: (check all that apply)

☑ Charge fee(s) indicated below

☐ Charge fee(s) indicated below, **except for the filing fee**

☑ Charge any additional fee(s) or underpayments of fee(s) under 37 CFR 1.16 and 1.17

☑ Credit any overpayments

to the above-identified deposit account.

☐ Other (please identify): _____

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FEE CALCULATION

1. BASIC FILING FEE

Fee Description	Fee ($)	Small Entity Fee ($)	Fee Paid($)
Utility Filing Fee	790	395	
Design Filing Fee	350	175	
Plant Filing Fee	550	275	
Reissue Filing Fee	790	395	
Provisional Filing Fee	160	80	

Subtotal (1) $ _____

FEE CALCULATION (continued)

2. EXTRA CLAIM FEES

Fee Description	Fee ($)	Small Entity Fee ($)
Each claim over 20	50	25
Each independent claim over 3	200	100
Multiple dependent claims	360	180
For Reissues, each claim over 20 and more than in the original patent	50	25
For Reissues, each independent claim more than in the original patent	200	100

Total Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 20 or HP =	_____	x _____	= _____

HP = highest number of total claims paid for, if greater than 20

Indep. Claims	Extra Claims	Fee ($)	Fee Paid ($)
_____ - 3 or HP =	_____	x _____	= _____

HP = highest number of independent claims paid for, if greater than 3

Multiple Dependent Claims	Fee ($)	Fee Paid ($)
	_____	_____

Subtotal (2) $ _____

3. OTHER FEES

Fee Description	Fee ($)	Small Entity Fee ($)	Fee Paid($)
1-month extension of time	120	60	
2-month extension of time	450	225	
3-month extension of time	1,020	510	
4-month extension of time	1,590	795	
5-month extension of time	2,160	1,080	
Information disclosure stmt. fee	180	180	
37 CFR 1.17(q) processing fee	50	50	
Non-English specification	130	130	
Notice of Appeal	500	250	
Filing a brief in support of appeal	500	250	500
Request for oral hearing	1,000	500	
Other: _____			

Subtotal (3) $ 500

SUBMITTED BY

Signature		Registration No. (Attorney/Agent) 47.159	Telephone 512.370.2832
Name (Print/Type)	Robert A. Voigt, Jr.		Date 03/15/2006

PTO/SB/21 (09-04)
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TRANSMITTAL FORM

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Total Number of Pages in This Submission: 25

Application Number	09/884,660
Filing Date	06/19/2001
First Named Inventor	Peter K. Chow
Art Unit	2663
Examiner Name	Chang, Richard
Attorney Docket Number	F1018

ENCLOSURES *(Check all that apply)*

- [x] Fee Transmittal Form
  - [ ] Fee Attached
- [ ] Amendment/Reply
  - [ ] After Final
  - [ ] Affidavits/declaration(s)
- [ ] Extension of Time Request
- [ ] Express Abandonment Request
- [ ] Information Disclosure Statement
- [ ] Certified Copy of Priority Document(s)
- [ ] Reply to Missing Parts/ Incomplete Application
  - [ ] Reply to Missing Parts under 37 CFR 1.52 or 1.53
- [ ] Drawing(s)
- [ ] Licensing-related Papers
- [ ] Petition
- [ ] Petition to Convert to a Provisional Application
- [ ] Power of Attorney, Revocation Change of Correspondence Address
- [ ] Terminal Disclaimer
- [ ] Request for Refund
- [ ] CD, Number of CD(s) _____
  - [ ] Landscape Table on CD
- [ ] After Allowance Communication to TC
- [ ] Appeal Communication to Board of Appeals and Interferences
- [x] Appeal Communication to TC **(Appeal Notice, Brief, Reply Brief)**
- [ ] Proprietary Information
- [ ] Status Letter
- [x] Other Enclosure(s) (please Identify below):
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Remarks

SIGNATURE OF APPLICANT, ATTORNEY, OR AGENT

Firm Name	Winstead Sechrest & Minick P.C.		
Signature			
Printed name	Robert A. Voigt, Jr.		
Date	03/15/2006	Reg. No.	47,159

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Typed or printed name	Toni Stanley	Date	03/15/2006

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